93000 SOC Series Model C200e

Data Sheet

The cost-optimized C200e model offers flexible configurations that address the broadest application coverage while providing the lowest cost of test. The C200e is a complete solution with everything you need to test starting at $399,000.

Offering the Lowest Price-Per-Pin in the Industry

The cost-optimized C200e model is a member of the 93000 single scalable platform that offers flexible configurations that address the broadest application coverage while providing the lowest cost of test. Single scalable platforms help you save time, money and reduce complexity of test. Optimized for low cost consumer and wireless applications requiring a platform for mixed signal functional testing who are constantly challenged with reducing their cost-of-test:

- **Wireless Communications**
- **Digital Consumer Solutions**
- **Computation, Chipsets, & Graphics Solutions**

Performance Scalability

The Agilent 93000 SOC Series gives you the right models to meet the challenges of SOC testing: Ce-models for cost-sensitive applications and P- and NP-models where performance is paramount. The SOC Series offers you an exceptional speed/accuracy performance range starting at an extremely low entry-level price. In addition to scalable analog, digital and RF, digital speeds from 200 Mbps up to 3.2 Gbps, the ability to mix digital channels between models with port scalability makes the Agilent 93000 SOC Series the ultimate in meeting your SOC test needs as they change over time. From test head size, to pins, ports and test capabilities, one scalable platform for all performance levels helps you to manage unpredictable market needs and consequently reduce risk.

Lower cost of test

The scalability and architecture of the Agilent 93000 SOC Series is the way to achieve the lowest COT. Because you can expand and upgrade the systems as required, you can invest when you need to, minimizing up-front

capital costs. Pay-Per-Use, Agilent's patented method for temporarily upgrading speed, gives you the freedom to do this immediately, as your needs change. Analog and RF capabilities are easily upgraded as well. But capital cost is only one aspect. Because the SOC Series can be configured to meet your needs for a wide range of devices, you reduce the overhead, that would otherwise be required to support a complex manufacturing infrastructure of multiple, incompatible testers. This means your operators, design and test engineers, as well as maintenance personnel, require less training and are more flexible. To ensure you even greater flexibility, Agilent offers a variety of financing programs to best meet your specific business needs.

System Options

The Model C200e is a member of the 93000 platform, ensuring full compatibility between systems, software, DUT boards, and mechanical docking. It can be configured to meet the needs of your application with the following Related Products:

- **Analog Modules**
- **RF Measurement Suite**
- **Digital Test**
- **CMOS Image Sensor Test Solution**
- **SmarTest Program Generator**

Features and Benefits

Features	Benefits
Test Processor-Per-Pin	• All test data stays local to the test processor, ensuring high digital performance and a low system noise floor • A sequencer-per-pin provides localized test execution, minimizing test time
Channel Mixing	• High-performance digital cards can be added as needed to create a cost-optimized system for high-speed interfaces and clocks, minimizing capital cost
Multi-Site Test	• Easily upgrade digital speed or vector memory to address new applications or the latest technologies, maximizing utilization • Invest when you need to, minimizing upfront costs and reducing cost-of-test
Concurrent Test	• With up to 1024 pins, the 93000 provides the high digital and analog pin count for multi-site test of highly integrated SOCs • A Test Processor-Per-Pin architecture, coupled with integrated analog modules, provides high parallel efficiency, maximizing throughput
X-Modes	• Higher speed • Vector compression • Better match to device cycles
Scan-Per-Pin	• Supports both the narrow-deep and the wide-shallow scan approaches • Scan chains run at full tester speed, minimizing test times with at-speed test
APG-Per-Pin for Embedded Memory Test	• Every digital pin can act as an APG (Algorithmic Program Generator) • APG runs up to the maximum sequencer speed of the system, minimizing test times with at-speed test

Key Specifications

Specification	Value
Number of Digital Pins	Up to 1024 pins (increments of 16)
Number of analog modules	24 max.
Number of device power supplies	8 max.
RF Measurement Suite	Up to 12 RF Ports
Number of digital pins	1024 max (increments of 16)
Digital data rate	250 Mbps at 1V
Digital Clock Rate	200 MHz at 3V
Edge placement accuracy (EPA)	175 ps
Overall timing accuracy (OTA)	350 ps
Memory per pin	56 MVector max.
Scan per pin	336 MVector max.

www.agilent.com
800 123-4567

Sales, Service and Support

Please note that contact information can vary in content from organization to organization. Please edit as needed.

United States
1 800 123 4567

Canada
1 877 **123 4567**
(905) **123 4567** (FAX)

Europe
(31 20) **123 4567**
(31 20) **123 4567** (FAX)

Japan
(81) **123 45 6789**
(81) **123 45 6789** (FAX)

Latin America
(305) 123 4567
(305) 123 4567 (FAX)

Australia
1 800 123 45 67 89
(613) 123 45 67 89 (FAX)

New Zealand
0800 123 456 78
64 123 456 78 (FAX)

Asia-Pacific
(852) 123 45 6789
(852) 123 45 6789 (FAX)

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